

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
a substrate;
one or more logic devices formed over the substrate, wherein at least one of the one or more logic devices comprises a high dielectric constant (high-k) gate dielectric; and
one or more memory devices formed over the substrate, wherein at least one of the one or more memory devices comprises a non-high-k gate dielectric.
2. The semiconductor device of claim 1 wherein the substrate comprises defective crystalline to accommodate logic devices with strained channel.
3. The semiconductor device of claim 1 wherein the k of the high-k gate dielectric is at least 20.
4. The semiconductor device of claim 1 wherein the k of the non-high k gate dielectric is less than 8.
5. The semiconductor device of claim 1 wherein the logic device comprises a metal-oxide semiconductor field-effect transistor (MOSFET).
6. The semiconductor device of claim 1 wherein the memory device comprises a dynamic random access memory (DRAM).
7. The semiconductor device of claim 1 wherein the memory device comprises a static random access memory (SRAM).
8. The semiconductor device of claim 1 wherein the memory device comprises a non-volatile memory.
9. The semiconductor device of claim 1 wherein the memory device comprises Electrically Programmable Memory (EPROM) or Electrically Erasable Programmable Memory (E2PROM).

10. The semiconductor device of claim 1 wherein the thickness of the high-k gate dielectric is less than about 50 Angstroms.

11. The semiconductor device of claim 1 wherein the thickness of the non-high-k gate dielectric is less than about 15 Angstroms.

12. The semiconductor device of claim 1 wherein the high-k gate dielectric comprises tantalum pentoxide.

13. The semiconductor device of claim 1 wherein the high-k gate dielectric comprises hafnium oxide.

14. The semiconductor device of claim 1 wherein the high-k gate dielectric comprises aluminum oxide.

15. The semiconductor device of claim 1 wherein the high-k gate dielectric comprises one of the following: titanium oxide, barium strontium titanate, zirconium oxide, hafnium silicon oxide, zirconium silicon oxide, hafnium aluminum oxide, zirconium aluminum oxide, and strontium titanium oxide.

16. The semiconductor device of claim 1 wherein the non-high-k gate dielectric comprises one of the following: silicon oxide, silicon nitride, and silicon oxynitride.

17. A semiconductor device, comprising:
a substrate;
a first gate dielectric over the substrate, wherein the first gate dielectric is for a logic device and comprises a high dielectric constant (high-k) material;
a second gate dielectric over the substrate, wherein the second gate dielectric is for a memory device and comprises a non-high-k material; and
and a gate electrode over the second gate dielectric.

18. The semiconductor device of claim 17 further comprising forming an insulating layer that comprises silicon nitride or silicon oxynitride under the first gate dielectric.

19. The semiconductor device of claim 17 wherein the first gate dielectric comprises hafnium oxide.

20. The semiconductor device of claim 17 wherein the first gate dielectric one of the following: tantalum pentoxide, titanium oxide, barium strontium titanate, zirconium oxide, hafnium silicon oxide, zirconium silicon oxide, hafnium aluminum oxide, zirconium aluminum oxide, and strontium titanium oxide.

21. The semiconductor device of claim 17 wherein the second gate dielectric comprises one of the following: silicon oxide, silicon nitride, and silicon oxynitride.

22. The semiconductor device of claim 17 wherein the substrate comprises silicon-on-insulator.

23. The semiconductor device of claim 17 wherein the substrate comprises silicon.

24. The semiconductor device of claim 17 wherein the substrate comprises silicon with defective crystalline.

25. The semiconductor device of claim 17 wherein the memory device comprises a stack-type dynamic random access memory (DRAM).

26. The semiconductor device of claim 17 wherein the memory device comprises a trench-type dynamic random access memory (DRAM).

27. The semiconductor device of claim 17 wherein the memory device comprises a dynamic random access memory (DRAM), static random access memory (SRAM), magnetic RAM, or non-volatile memory.

28. The semiconductor device of claim 16 wherein the memory device comprises Electrically Programmable Memory (EPROM) or Electrically Erasable Programmable Memory (EEPROM).

29. The semiconductor device of claim 16 wherein the logic device comprises a metal-oxide semiconductor field-effect transistor (MOSFET), wherein the MOSFET comprises a channel in <100> crystalline direction.

30. The semiconductor device of claim 16 wherein the logic device comprises an electrically conductive gate electrode, wherein the electrically conductive gate electrode is selected from the group consisting of: metal, metal silicide, metal nitride, metal alloy, and a metal compound.

31. The semiconductor device of claim 16 wherein the logic device comprises an electrically conductive gate electrode, wherein the electrically conductive gate electrode comprises titanium nitride.

32. The semiconductor device of claim 16 wherein the logic device comprises an electrically conductive gate electrode, wherein the width of the electrically conductive gate electrode is less than 900 Angstroms.

33. The semiconductor device of claim 16 wherein the memory device comprises a gate electrode, wherein the gate electrode comprises metal silicide or polysilicon.

34. The semiconductor device of claim 16 wherein the memory device comprises a gate electrode, wherein the width of the gate electrode is less than 1300 Angstroms.

35. A method for semiconductor manufacturing, comprising:
providing a substrate;
forming a first gate dielectric with a high dielectric constant (high-k) material, wherein the first gate dielectric is for a logic device; and
forming a second gate dielectric with a non-high-k material, wherein the second gate dielectric is for a memory device.

36. The method of claim 35 wherein the high-k gate dielectric comprises tantalum pentoxide.

37. The method of claim 35 wherein the high-k gate dielectric comprises hafnium oxide.
38. The method of claim 35 wherein the high-k gate dielectric comprises aluminum oxide.
39. The method of claim 35 wherein the high-k gate dielectric is selected from the group consisting of: titanium oxide, barium strontium titanate, zirconium oxide, hafnium silicon oxide, zirconium silicon oxide, hafnium aluminum oxide, zirconium aluminum oxide, and strontium titanium oxide.
40. The method of claim 35 further comprising forming an insulating layer that comprises silicon nitride or silicon oxynitride under the first gate dielectric.